WHAT IS CLAIMED IS:

1. A method for managing latency comprising:

receiving data from a high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-order tributary unit (TU) and virtual tributary (VT) sources;

providing a provisioning bit for each output associated with a memory; and

adjusting a pointer for the low-order sources based on the provisioning bit such that the high-order and low-order outputs are synchronized.

2. The method of claim 1 further comprising determining an adjustment for the pointer based on a predetermined delay.

3. The method of claim 1 wherein adjusting the pointer includes adjusting the pointer by a predetermined number of time slots.

4. The method of claim 1 further comprising

assembling synchronized outputs from the memory.

5. The method of claim 1 further comprising

adjusting the pointer to synchronize the output of the high-order and low-order sources, wherein the high-order sources incur less delay to pass through the memory than low-order sources.

6. The method of claim 1 wherein providing a provisioning bit includes storing the provisioning bit in a connection memory.

7. The method of claim 1 wherein adjusting a pointer for the low-order sources based on the provisioning bit includes adjusting the pointer when the provisioning bit is set.

8. The method of claim 7, further comprising setting the provisioning bit for low-order sources.

9. The method of claim 1 wherein adjusting a pointer for the low-order sources based on the provisioning bit includes not adjusting the pointer when the provisioning bit is not set.

10. The method of claim 9 further comprising setting the provisioning bit for high-order sources.

11. A computer program product tangible embodied on a computer readable medium, for provisioning cross-connects in network switching environment comprising instructions for causing a computer to:

receive data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-order tributary unit (TU) and virtual tributary (VT) sources;

provide a provisioning bit for each output associated with a memory; and

adjust a pointer for the low-order sources based on the provisioning bit such that the high-order and low-order outputs are synchronized.

12. The computer program product 11 further comprising instructions for causing a computer to:

determine an adjustment for the pointer based on a predetermined delay.

13. The computer program product of claim 11 further comprising instructions for causing a computer to:
adjust the pointer by a predetermined number of time slots.

14. The computer program product of claim 11 further comprising instructions for causing a computer to:
assemble synchronized outputs from the memory.

15. The computer program product of claim 11 further comprising instructions for causing a computer to:
adjust the pointer to synchronize the output of the low-order and high-order sources, wherein the high-order sources incur less delay to pass through the memory than low-order sources.

16. The computer program product of claim 11 further comprising instructions for causing a computer to:
store a provisioning bit in a connection memory.

17. The computer program product of claim 11 further comprising instructions for causing a computer to:
adjust a pointer for the low-order sources based on the provisioning bit includes adjusting the pointer when the provisioning bit is set.

18. The computer program product of claim 11 further comprising instructions for causing a computer to:

adjust a pointer for the low-order sources based on the provisioning bit includes not adjusting the pointer when the provisioning bit is not set.

19. An apparatus including:

a memory for storing a provisioning bit for each output associated with a memory;

a first circuit configured to receive data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-order tributary unit (TU) and virtual tributary (VT) sources;

a second circuit configured to adjust a pointer for the low-order sources based on the provisioning bit such that the high-order and low-order outputs are synchronized.

20. The apparatus of claim 19 wherein the second circuit is configured to adjust the pointer by a predetermined number of time slots.

21. The apparatus of claim 19 wherein the second circuit is configured to adjust the pointer to synchronize the output of the high-order and low-order sources, wherein the high-order sources incur less delay to pass through the memory than low-order sources.

22. The apparatus of claim 19 wherein the memory is a connection memory.